1. A method for making a dielectric structure for dual-damascene applications, the method comprising:

providing a substrate;

fabricating metallization lines within the substrate;

forming a barrier layer over the metallization lines and the substrate;

forming an inorganic dielectric layer to define a via dielectric layer over the barrier layer, the inorganic dielectric layer being highly selective relative to the barrier layer when etched; and

forming a low dielectric constant layer to define a trench dielectric layer over the inorganic dielectric layer.

2. A method for making a dielectric structure for dual-damascene applications as recited in claim 1, further comprising:

forming a trench in the low dielectric constant layer using a first etch chemistry.

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3. (Amended) A method for making a dielectric structure for dual-damascene applications as recited in claim 2, further comprising:

forming a via in the inorganic dielectric layer using a second etch chemistry, the second etch chemistry being different than the first etch chemistry and the via being within the trench.

4. A method for making a dielectric structure for dual-damascene applications as recited in claim 1, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

5. A method for making a dielectric structure for dual-damascene applications as recited in claim 4, wherein the forming of the inorganic dielectric layer includes,

depositing a TEOS silicon dioxide material over the barrier layer.

6. A method for making a dielectric structure for dual-damascene applications as recited in claim 5, wherein the forming of the low dielectric constant layer includes,

depositing a carbon doped oxide.

7. A method for making a dielectric structure for dual-damascene applications as recited in claim 3, wherein the inorganic dielectric layer is one of a TEOS oxide layer and a fluorine doped oxide layer, and the low dielectric constant layer is a carbon doped oxide layer.

8. A method for making a dielectric structure for dual-damascene applications as recited in claim 7, wherein the first etch chemistry is optimized to etch through the carbon doped oxide layer and the second etch chemistry is optimized to etch through the TEOS oxide layer or the fluorine doped oxide layer.

9. A method for making a dielectric structure for dual-damascene applications as recited in claim 8, wherein the second etch chemistry is selective to the barrier layer.

10. A method for making a multi-layer inter-metal dielectric over a substrate, comprising:

forming a barrier layer over the substrate;

forming a silicon dioxide layer over the barrier layer;

forming a low dielectric constant layer over the silicon dioxide layer;

forming a trench through the low dielectric constant layer; and

forming a via in the trench extending through the silicon dioxide layer to the barrier layer.

11. A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 10, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

12. A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 11, wherein the forming of the silicon dioxide layer includes, depositing one of an un-doped TEOS oxide layer and a fluorine doped oxide layer.

13. A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 12, wherein the forming of the low dielectric constant layer, includes, depositing one of a carbon doped oxide layer and an organic dielectric layer.

14. (Amended) A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 10, wherein forming the via in the trench extending to the barrier layer further includes,

implementing a first chemistry optimized to etch through the low dielectric constant layer; and

implementing a second chemistry which is different than the first etch chemistry and is optimized to etch through the silicon dioxide layer.

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15. A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 14, wherein the second chemistry that is optimized to etch through the silicon dioxide layer is selective to the barrier layer.

16. A method for making a multi-layer inter-metal dielectric over a substrate as recited in claim 15, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

TSP1P99/102 26 26. A method for making a multi-layer intermetal dielectric over a substrate as recited in claim 10, further comprising:

etching the barrier layer; and

forming a via and trench barrier layer to cover a surface within the via and the trench,

wherein the via and trench barrier layer is one of tantalum nitride material and tantalum material.

REMARKS

The Examiner is thanked for the careful review of this application. Claims 1-16 and 26 are pending after entry of this Amendment. Claims 3 and 14 are herein amended. The claims are amended to clarify the present application. The Examiner is referred to the Applicants' specification as filed, page 11, line 22 – page 12, line 22 for support of the claim amendments. No new matter is introduced.

Rejections under 35 U.S.C. §112

Claims 1-16 and 26 were rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter